ISBN: 978-3-95450-241-7 ISSN: 2673-5350 doi:10.18429/JACoW-IBIC2022-TUP42

FAST ORBIT FEEDBACK UPGRADE AT SOLEIL

R. Broucquart†, N. Hubert, Synchrotron SOLEIL, Gif-Sur-Yvette, France

Abstract

In the framework of the SOLEIL II project, the diagnostics group must anticipate ahead of the dark period the upgrade of important system like the BPM electronics, the timing system end the Fast Orbit Feedback (FOFB). The FOFB is a complex system that is currently embedded in the BPM electronics modules (eBPM). A new flexible stand-alone platform is under conception to follow the future upgrades of surrounding equipment, and to allow the integration of future correction schemes. In this paper we will present the current status of technical decisions, tests and developments.

CONTEXT

SOLEIL II aims at outstanding performances on the beam physics, qualified with renewed instrumentations. Most of the equipment linked to the FOFB will have to be updated to either accommodate these new performances (corrector magnets and their power supplies) or because they have reached obsolescence (BPM electronics, timing system).

The eBPMs (Libera Electron) currently host a major part of the FOFB system: 1) they are linked with a fast dedicated network to exchange the measured positions in all bpm location, 2) they compute the correction to apply from the given response matrix and 3) they communicate with the corrector magnet Power Supplies Controller (PSC) to apply the correction on beam.

These features have been embedded in the FPGA located inside those electronics. Most are custom developments or integration of the Diamond Light Source Communication Controller (DLS CC) [1]. This entanglement makes it difficult to upgrade the eBPMs, having to deal with two major applications: position monitoring and FOFB.

As FOFB system are very dependent on the machine layout, boundary systems and stabilization strategy, it has been decided to keep this system as an in-house development. To ease the integration, our strategy is to first segregate the FOFB system on a new dedicated platform. This platform will be interfaced with current eBPMs, PSC and timing system. It will evolve with the upgrade of each of these boundary systems.

On a feature perspective, the initial goal is to reproduce the actual features, operation control interface and performances. Future features will then be added: augmented monitoring, special mode of operation for fast lattice parameters measurements, new correction scheme… With the evolution of boundary systems and features in mind, a new modular FOFB system has been proposed.

† romain.broucquart@synchrotron-soleil.fr

SPECIFICATIONS AND GOALS

- Functionalities reproduced: With the new FOFB system platform, obtain the same service as provided currently.
- Increased performances: Communication latency and data rate will be improved, and with the leverage of a reduced latency of the future eBPMs, it will unlock a larger correction bandwidth. Performances evolution are given in Table 1.
- Follow machine evolution: SOLEIL II will bring down beam dimensions and thus stability requirements. With new correctors magnets and power supplies, the FOFB system shall attain lower stability dimensions.
- Offer new features: The new platform will allow new monitoring and fast lattice parameters measurement, such as fast response matrix identification or fast beam based alignment.

Table 1: FOFB Performances Evolution

	Actual FOFB	Future FOFB
# BPM	122	~180
# Corrector	50 H & V	*To be defined*
Data rate	10 kHz	100 kHz
Correction BW	150 Hz	1 kHz
Latency (communication and computation)	100 µs	10 µs
Stability	10 % of beam size 20 µm H ; 0.8 µm V	5% of beam size 50 nm H & V

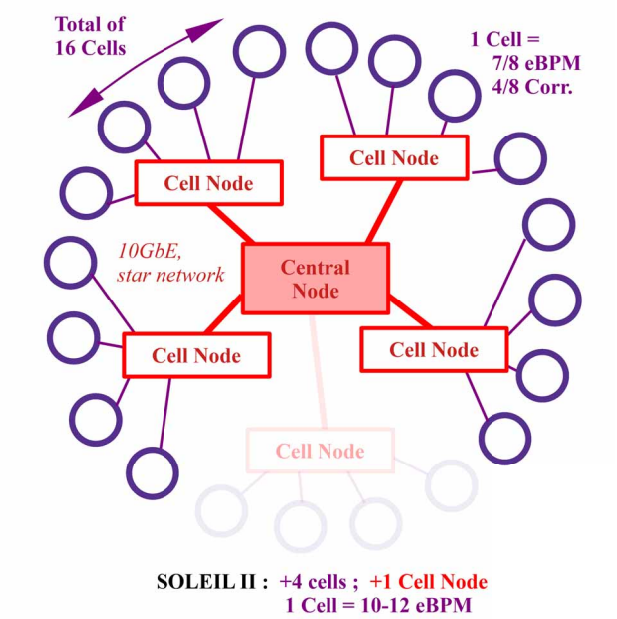

Figure 1: Network Topology.

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ROPOSED SYSTEM

The proposed system is supported by several hardware platforms linked in a dedicated network. In the following section we will present technical choices for every aspect of the system.

Dedicated Network

The FOFB system is at the interconnection of multiple eBPMs and PSCs, all scattered in the synchrotron building. On the current system [2], all Libera Electron are linked to 2-3 neighbours, making a redundant ring network. This topology naturally provides redundancy, but the communication latency grows with the number of endpoints. The ring topology is efficient for the current implementation of the correction computation, with a distributed matrix multiplication which may not be possible for future correction schemes. For the new system, we envision that a centralized computation will ease the implementation of features such as the interface with Slow Orbit Feedback, complex controller or correction scheme adaptability to injection event.

A star topology naturally provides a central node that connects to every end points. We will use this topology for our core network made of a Central Node and 4 Cell Nodes as shown in Fig. Error: Reference source not found. The direct fast connexion between the Central Node and Cell Nodes will be the backbone of the network, with a protocol independent of the boundary systems. For this protocol, we selected to forge custom packets encapsulated in Ethernet MAC frames, running on a 10GbE fiber link. As SOLEIL II increases the number of endpoints (eBPMs and PSCs), we can extend the network by adding one Cell Node.

The selection of an Ethernet based protocol enable us to use on the shelf solution if required, such as network switches. While Ethernet is not originally aimed at low latency, it provides proved robustness and basics features that we require. We do not use a full TCP/UDP and IP stack, as we do not require generic routing and addressing. Frames structures are defined in Fig. 2. As single Ethernet frame can contain up to 149 position data or 248 correction data and will be carried in around 1.2 µs over a 10GbE link.

Cell Nodes will be connected to the boundary systems using the interface required by them. Cell Nodes act as gateway in our network, aggregating data packets from the eBPMs and dispatching correction packets to PSCs. The topology of this outer network depends on the solution used for eBPMs and PSCs. For the first phase, Cell Nodes will simply tap in the eBPM ring network and will be connected directly to the PSCs, keeping the same communication latency. With new eBPMs, we can assume a 1 Gbps link between a Cell Node and eBPMs. This leads to a transmission time of a little above 1 µs for 12 eBPMs aggregated over the same interface (10 bytes per eBPM, no overhead considered).

Redundancy is not naturally covered by this new topology. On the current FOFB system, rare optical fiber connexion incident can occur, solved by restarting the SFP modules. The new topology will be more vulnerable to this kind of problem. It can be tempered for example by opting for high grade SFP modules, or running two parallel connexion (cold or hot swap). To minimize the down time, automatic routine can be developed to restart the module and restart the system faster.

Hardware Platform

For development and maintenance simplicity, we aimed at an identical platform for the Cell Nodes and Central Node. The Micro TCA standard (MTCA) is common in accelerator facilities. This standard allows a very good flexibility: chassis size and complexity, vast selection of AMC board, adding custom RTM board.

For our application, we selected the DAMC-FMC2ZUP board [3]. It mainly features 2 FMC slots with 16 and 8 transceivers – giving us flexibility on interfaces – and a Zynq Ultrascale+ SOC – providing FPGA and CPU supports. As this AMC board provide enough resources alone, we selected a small, cost-efficient MTCA chassis [4] to host it.

For communication with current eBPMs and central node, we selected a 4SFP+ FMC [5] as we only need a few. This solution can be upgraded by doubling it and/or increasing the number of interfaces with double QSFP+ or MPO interfaces.

For communication with the current PSCs, we need up to 32 serial interfaces per Cell Node. Given the very high density, the simplicity of the interfaces and the short life span of this solution, we chose to design a custom RTM board, named CACTUS. This board simply contains RS422 drivers connected to the AMC board and RJ45 connectors. Simple CAT5 cables will carry signals on 4 differential pairs, routed to cell racks and split there. In the future, the communication to the SOLEIL II PSCs will

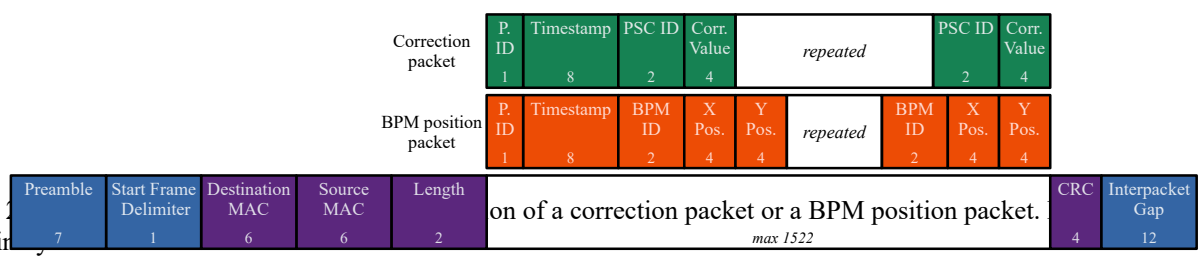

Figure 2
given in

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be move to a high speed – low latency – protocol and interface. The CACTUS board will be then removed.

The DAMC-FMC2ZUP also provides a high density interface for timing. It can accept clock & trigger LVDS signals – compatible with the current local cell timing distribution at SOLEIL – or it also provides compliance with White Rabbit timing distribution – a possible candidate for SOLEIL II.

The platform obtained can be upgraded for still unspecified usages: integration of XBPM is foreseen, the interface to future PSC is still unknown. These usage will be supported by either increasing the number of SFP+ interfaces, or using a new FMC, AMC or RTM board.

In case of a platform failure, the orbit stability is degraded until the platform is replaced by a spare. As the platform is composed of several modules, the reparation can be eased by replacing only the defective part. The total cost of the hardware platform amount to about 12k€.

FPGA Firmware

A lot of functionalities will be embedded in the FPGA matrix of the SOC: high speed communication, correction computation, data capture… These functionalities will evolve with the FOFB system and the boundary systems.

To stir the development to a maintainable and evolutive format, we decided to use the FWK project framework developed by DESY MSK [6]. This cut down big project into modules, adding automation to organize, test, build and reproduce. Choosing FWK also provides good compatibility with ChimeraTK (presented in next section), and allows block exchange with other facilities using this framework.

The main modules used in our project are represented in Fig. 3 and listed below (not exhaustive, development under progress).

- COMBPM: receive and decode the eBPM data stream. It translates the BPM frames to AXI4-Stream packets. It provides packet filtering. For now, it only aims at decoding Libera Electron DLS CC stream, but it will be completed with the required capacity for the future eBPMs.
- COMCELLNODE: data exchange based on 10GbE MAC and PHY. Additional modules prepare BPM and correction packets to encapsulate in MAC frames, or decapsulate them for local processing.
- COMCORR: Route and encode correction data to the destination PSC. As for the COMBPM module, this module will evolve with future PSCs.
- CORRECTION: Apply the correction algorithm on the BPM data to obtain the correction data.
- TIMING: Receive clock and trigger and maintain a local time synchronized with the machine clock (turn by turn clock).

Using the widely known AXI4-Stream for data stream and AXI4 Memory Mapped for register access enable us to leverage generic IP such as AXIS interconnects.

The main challenge encountered so far was the configuration of the transceivers, because one quad is affected with two very different protocols, which require a custom configuration of the QPLL (Quad PLL).

Software Stack

SOLEIL II will keep Tango as the Control System. Current operation of the FOFB is piloted from Matlab GUI, which interact on a main Tango device dispatching configuration and retrieving status of all eBPMs and PSC Tango devices.

To keep up with the FOFB system evolution, we are in the process of deploying a very flexible software stack. The CPU part of the SOC runs an embedded Linux, which we will leverage to host services for control. We aim at using ChimeraTK [7] to build an OPCUA server, offering remote access to control and status registers of the FPGA modules.

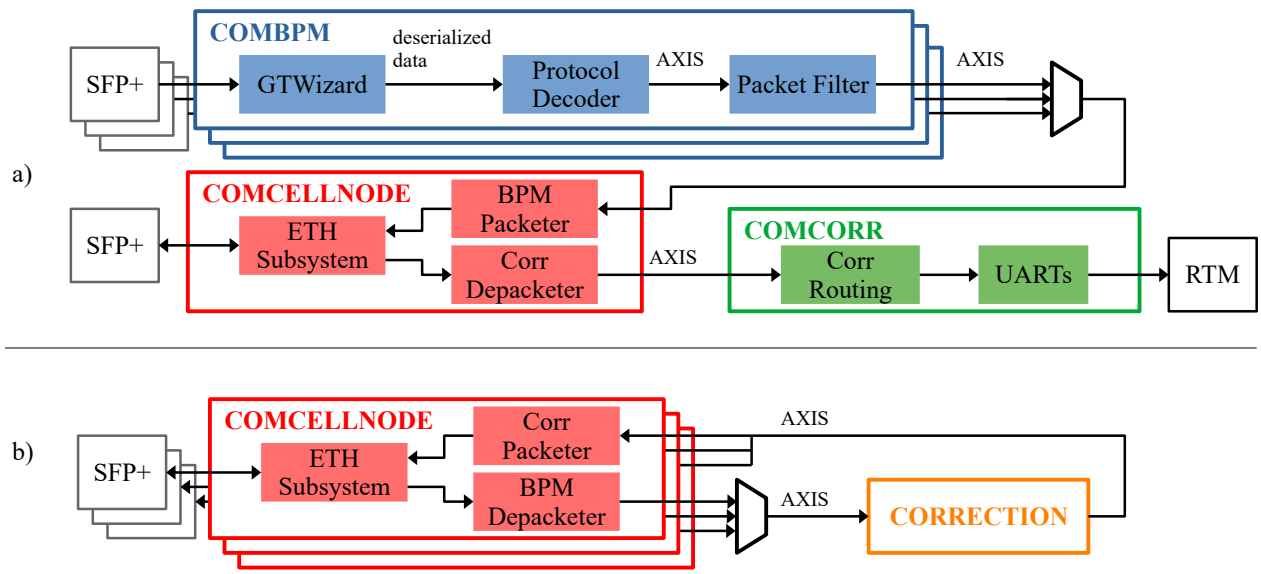

Figure 3: Overview of FPGA firmware modules for a) Cell Nodes and b) Central Node

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This on-board OPCUA server will be contacted from a generic Tango device server, acting as a OPCUA client. This will allow very simple access from SOLEIL control system to the FPGA modules. When changing the FPGA registers, this whole software stack can be quickly updated with map files, without requiring compilation.

For important data captures – i.e. hundreds of points, for identification measures or debug – we aim at using Direct Memory Access (DMA) to move the data in the AMC DDR. Another service – still to be defined – will then operate an upload to remote storage or allow a download from a client.

PROJECT STATUS

Despite the strain on electronic productions chains, we now gathered all the platforms for operation. Prototyping and tests were already run on a first platform.

- Communication with eBPM was validated in lab, then by taping in the real network. As we only read the data stream, we are able to capture data during normal operation.
- 10GbE was validated in lab, with loopbacks at transceivers and cable. Additional tests were made with an Ethernet switch [8], mainly to measure the minimal latency obtain with such device, but it also cross-check our Ethernet interface (signals and frame) with a commercial solution.
- Communication with current PSC was validated in lab, using a RS422 FMC board.
- Timing signals – clock and trigger – from our current Cell local board were correctly used in lab.
- We also integrated a double QSFP+ board to validate the possibility to increase interface density.

The custom RTM board will be under test from September 2022. A small network of 1 Cell Node and 1 Central Node will be deployed on the running eBPM network by the end of 2022. It will run in open loop (not driving actual PSCs). During 2023, this network will be then increased to its full size and real scale test with closed loop will take place during machine test runs. We aim at an operational status by summer 2023. Next major step dates depend on boundary systems evolutions.

CONCLUSION

The new FOFB is under development at SOLEIL, getting from prototype to a first version. As the system is found at the intersection of several applications and systems, all expected to change, we opted for a very flexible platform. To manage integration with specific equipments and SOLEIL control system, his project requires hardware, FPGA and software developments.

ACKNOWLEDGEMENTS

We would like to thank J. Bisou, A. Bence, G. Pichon, S. Zhang, Y.M. Abiven and F. Bouvet from SOLEIL for their work or views on the project.

We equally thank C. Guemues, L. Butkowski and M. Killenberg from DESY for their help with FWK and ChimeraTK.

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