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RF SYSTEM-ON-CHIP FOR MULTI-BUNCH AND FILLING-PATTERN FEEDBACKS*

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Abstract

We have evaluated an RF System-on-Chip (RFSoC) as a platform to implement the multi-bunch (bunch-by-bunch) feedback and the filling pattern (single bunch charge) measurement system for the Swiss Light Source (SLS) upgrade project, the SLS 2.0. This paper presents the status and first results of a preliminary design of the feedback systems using an RFSoC evaluation board, including test measurements at the SLS.

INTRODUCTION

The Swiss Light Source (SLS) is a synchrotron light source at Paul Scherrer Institute (PSI), and it has been in user operation since June 2001. The SLS beamlines cover research areas such as, but not exclusively, atomic and molecular science, material science, environmental and earth science, and life and medical science. To preserve the high scientific output of SLS, PSI plans an upgrade of SLS, the SLS 2.0. The SLS storage ring will be replaced, and an innovative magnet lattice with reverse bends will provide up to 60-fold higher brightness for hard X-rays [1]. Moreover, aging systems of the SLS will be exchanged, including the storage ring multi-bunch feedback (MBFB) and filling pattern feedback (FPFB). In this context, an RF System-on-Chip (RFSoC) from Xilinx/AMD [2] has been evaluated as a possible solution to substitute the existing technology of the MBFB and FPFB systems in operation at the SLS [3, 4]. The RFSoC integrates multi-core CPUs, FPGA fabric, high-speed analog-to-digital (ADC), and digital-to-analog data converters (DAC) with several Giga-samples per second (Gs/s) on a single chip. We have used the ZCU111 kit from Xilinx/AMD to evaluate the RFSoC [2]. The ZCU111 evaluation board features an RFSoC with eight 12-bit 4 Gs/s ADCs, eight 14-bit 6.5 Gs/s DACs, a 4-core 64-bit, and a 2-core 32-bit ARM CPU. In addition, the RFSoC provides various data storage and communication interfaces, including multi-gigabit links and Ethernet.

The following sections of the paper describe the implementation of a three-dimensional multi-bunch feedback (MBFB) and the measurement of the relative charge in each bunch (filling pattern) at the SLS storage ring with the RFSoC, using RF beam position monitor (BPM) signals.

HARDWARE

Figure 1 shows the hardware setup installed in the SLS storage ring for developing and testing the MBFB and filling pattern measurement using the RFSoC. A BPM with four capacitive button electrodes is connected to RF hybrids, generating: The sum signal, S, proportional to the bunch charge; the horizontal, X, and vertical, Y, signals proportional to the product of transverse bunch position offset and charge. The ZCU111 is the core component of the system. The device acquires and samples the X, Y, and S signals with its ADCs, and generates the correction signals with its DACs. The correction signals are amplified and drive the MBFB kickers. In addition, acquired signal S is used to measure the filling pattern.

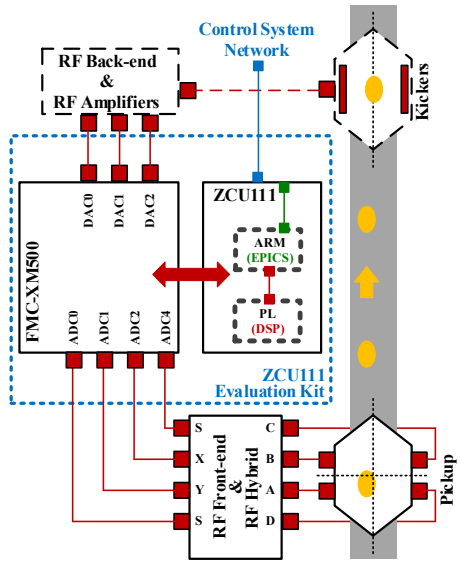

Figure 1: Hardware block diagram of the RFSoC-based multi-bunch feedback and filling pattern measurement.

The current MBFB system at SLS, presented in [3], has been in operation since 2006. The system has a commercial RF front-end (RFFE), which mixes the BPM signals from 1.25-1.5 GHz range down to baseband. The RFFE provides to ADCs: The transverse position signals, X and Y, and the phase signal for the longitudinal position, S. The signals X, Y, and S are sampled each by an 8-bit 500 Mega-samples per second (Ms/s) ADC. The signals are processed on a Virtex-2 FPGA with firmware implemented in VHDL at PSI. The driving signals for the transverse and longitudinal MBFB kickers are generated each by an 8-bit 500 Ms/s DAC. Each DAC directly drives the RF power amplifiers of transverse strip line kickers for X and Y channels. The longitudinal plane has an analog upconverter to transform the baseband (0-250 MHz) DAC signal to 1.25-1.5 GHz for the power amplifier of the longitudinal kicker.

The primary goal of the first MBFB implementation on the RFSoC was to facilitate the comparison with the current SLS system. Therefore, the new RFSoC firmware is functionally compatible with the analog signal conditioning of the current system. Consequently, the new and existing MBFB system electronics can be exchanged or even operated in parallel, enabling live switching between the two systems using combiners/splitters.

At SLS, the current FPFB measures the bunch charge with an avalanche photodiode (APD), using synchrotron

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radiation photons in the visible range [4]. The APD signal is digitized in oversampling mode with a VMEbus ADC board at 500 Ms/s. Embedded real-time software calculates the filling pattern using the acquired signals during the interval between the injections of consecutive top-up injection cycles. The filling pattern information is used to sort the electron bunches by charge. Finally, the sorted bunch indices are used to control the injections of the next top-up cycle. There are typically 15 single-bunch injections of 0.15 nC each at 3 Hz every few minutes. The FPFB fills at first bunches with the largest charge deficit from the user-defined filling pattern, and keeps the SLS ring beam current of usually 400 mA within a window of typically 2 mA.

In contrast to the RFSoC-based MBFB, the new filling pattern measurement with the RFSoC uses direct sampling of the BPM sum signal, S, without any analog signal preconditioning. Moreover, a unique firmware realizes both systems on the ZCU111 board.

FIRMWARE AND SOFTWARE

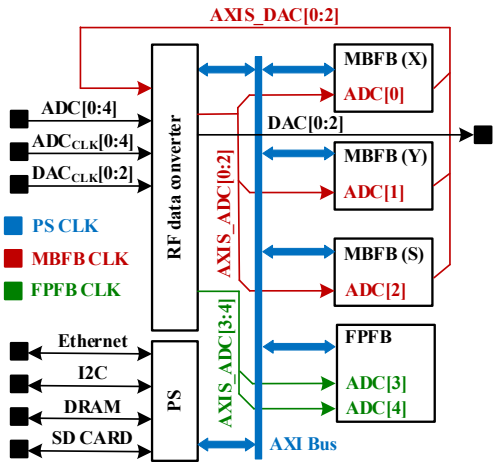

Figure 2: Firmware block diagram of the RFSoC-based multi-bunch feedback and filling pattern measurement.

Figure 2 shows the firmware block diagram of the systems on the RFSoC. The MBFB and the FPFB cores implement the multi-bunch feedback and the data acquisition for the FPFB, respectively. The central IP core of the design is the Xilinx RF Data Converter, which configures the ADCs and DACs and instantiates their interfaces to the programmable logic (PL) [2]. The ADC and DAC data are streamed from/to the AD/DA RF Data Converter core via AXI stream interfaces. The processing system (PS) core instantiates the ARM CPUs. The Ethernet interface of the PS communicates with the control system via an EPICS IOC running on the ARM CPU of the RFSoC. The AXI bus connects the PS to other IP Cores of the design. The I2C bus is used to control the peripherals of the ZCU111, including on-board PLLs that define the clock frequencies of the PL and sampling frequencies of the data converters. The ZCU111 uses the SLS machine reference clock of the ring central RF systems (f_{RF} = ~500 MHz). The clocks of the data converters and PL are synchronized to this reference clock and thus to the electron beam revolution frequency.

The ADCs and DACs 0 to 2 of the RFSoC, used for the MBFB, run at 8 × f_{RF} (~4 Gs/s), the red clock network in Fig. 2. The harmonic number of the SLS ring is 480. Thus, the ADC and DAC acquire eight samples per bunch and $N = 8 \times 480$ samples per storage ring revolution. Moreover, the ADC and DAC tiles of the RFSoC are configured in multi-tile synchronization (MTS) mode to guarantee temporal sample alignment among ADCs and DACs, as well as a reproducible latency from ADC to DAC after a power cycle of the system [2]. The ADCs 3 and 4, used for the FPFB, operate at a different clock (close to 4 Gs/s), the green network in Fig. 2. So that an interleaving scheme increases the effective sampling rate of these ADCs. The sampling frequency f_S is set to acquire a fractional number of samples per beam turn

$$f_s = \frac{f_{RF} \times 8 \times (M \times N - 1)}{(N \times M)}, \quad (1)$$

where N is the number of samples per beam turn, and M is the interleaving factor. The data, acquired over M turns, is interleaved, resulting in a waveform with M-fold higher effective sampling rate. In the prototype system, M is set to 16, providing an effective sampling rate of ~ 64 Gs/s.

Multi-bunch Feedback (MBFB) Systems

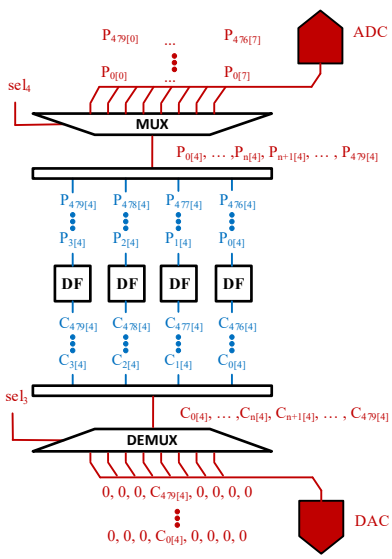

Figure 3: Data processing path of the MBFB System.

Figure 3 shows the signal processing path for the three MBFB planes. The interface between ADCs and PL operates at f_{RF} (~500 MHz), providing eight samples in parallel. Next, the 8 × f_{RF} (~4 Gs/s) data stream is decimated to 500 Ms/s by selecting one out of 8 samples, P_i, of the position signal. The resulting 500 Ms/s data stream is demultiplexed four times, generating four streams with 125 Ms/s for easier timing closure of the FPGA firmware. The bunch position P_i of each bunch is processed by digital filters (DF), resulting in the bunch correction signal C_i. In the output stage, the user can choose, with 250 ps resolution, when to apply the bunch correction signal C_i to kick the bunch with index i, b_i. Figure 4 shows the digital signal processing paths for the longitudinal (4a) and the two transverse (4b) planes of the MBFB. The IIR filters, gain stages,

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and generic FIR filters can be reconfigured to damp coherent bunch oscillations. For the prototype, the DF used in the longitudinal and transverse planes of the MBFB system is functionally equivalent to the filters presented in [3].

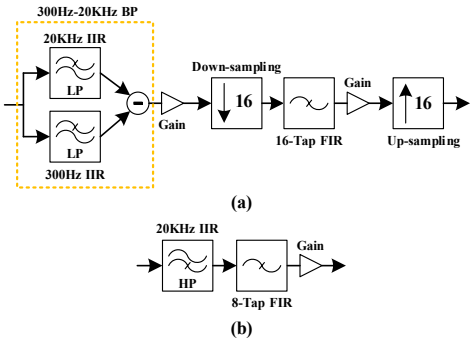

Figure 4: Block diagram of the digital filters for the longitudinal (a) and transverse (b) planes of the MBFB.

Filling Pattern Feedback (FPFB) System

The firmware of the test implementation of the FPFB using the RFSoC system consists of data acquisition blocks, which record the input data stream of ADCs 3 and 4, shown in Fig. 2. ADC 3 samples the revolution clock (reference for bunch indexing) and ADC 4 the sum signal, S (providing bunch charge and bunch arrival-time information). The acquisition core supports automatic trigger detection by level or external triggering, storing up to 512k samples for all ADC channels. Moreover, data can be acquired continuously or in multiple segments with user-defined length and inter-segment gaps. The communication and configuration of the acquisition core are done via AXI bus. The recorded data and configuration parameters can be accessed via EPICS channels.

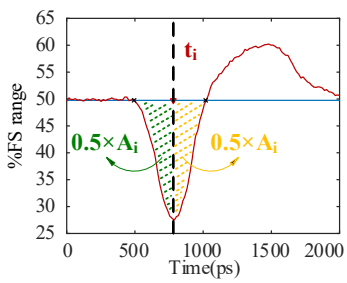

Figure 5: Sum signal, S, for one bunch windows of 2 ns, illustrating a single bunch pulse of the bunch train. The area A_i between the negative pulse (red curve) and the baseline (blue curve) is used to estimate the charge of the bunch b_i. Time t_i, which splits A_i in two equal parts, is an estimate for the arrival time of b_i.

The bunch charge and arrival time have been calculated offline on a PC in Python, with the acquired BPM data from the EPICS IOC running on the RFSoC. This first approach provided the flexibility to test different algorithms for the final version, which will be deployed in firmware/real-time embedded software.

Figure 5 shows a single bunch pulse from the sum signal, S. Each bunch window is 2 ns long, where A_i is the area between the negative pulse, red curve, and the baseline, blue curve. The baseline is the mean value of S in the bunch window. The charge of each bunch b_i is equal to a common factor k times the calculated area A_i. The bunch index i is assigned such that bunch zero is the first bunch after the revolution clock, and bunch 479 is the last before a new turn. The bunch arrival time of b_i is the time t_i, which splits the area A_i equally by two.

STATUS AND OUTLOOK

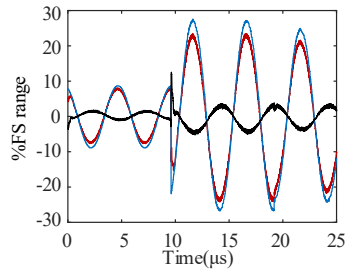

Figure 6: Hardware (red curve) and expected response (blue curve) of the transverse MBFB system (X-plane) for an arbitrary input. The black curve corresponds to the absolute error of the hardware response.

Multi-bunch Feedback (MBFB) Systems

The present prototype of the MBFB system has been designed to be functionally equivalent to the existing MBFB, aiming to evaluate if the RFSoC technology suits the application. In the first step, we verified that the latency from ADC to DAC of the RFSoC is reproducible after a power cycle of the ZCU111. While the old system has an external clock shifter, the RFSoC system latency can be adjusted on-chip in steps of 250ps via EPICS. Next, the data processing functionality of the MBFB was verified by firmware simulation and by feeding generated test signals into the new hardware and comparing the response to a software reference model. Figure 6 illustrates the functional verification of the MBFB system, showing the hardware and the expected response for the horizontal plane. Attenuation along the analog signal path leads to the difference between the two responses. Beam tests of the MBFB are planned for the following months. First, a one-to-one replacement of the present MBFB hardware with the new hardware is intended, keeping the analog down/up converters of the old system. Next, the external analog up converter for the longitudinal kicker will be removed, and the RFSoC will directly synthesize the kicker drive waveform (up to 1.5 GHz for SLS and 1.75 GHz for SLS 2.0). In addition, replacing the present analog downconverter RF front-end (RFFE) for the BPM signals is planned. For the new RFFE, we consider directly sampling the BPM signals with suitable signal bandwidth, gain and delay adjustment, aiming to process all ADC signals at the full sample rate of 4 Gs/s. Moreover, we are evaluating the option to digitally calculate X, Y, and S from the four button signals.

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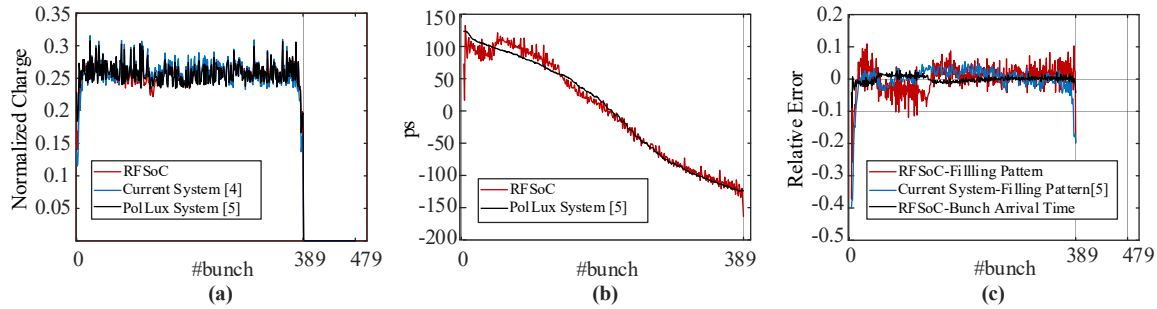

Figure 7: Measurements of the bunch (a) charge and (b) arrival time in the SLS. (c) Relative error of the bunch charge and arrival time measurements using a soft X-ray photon counting system of the SLS PolLux beamline as reference [5].

For SLS 2.0, we consider implementing more advanced diagnostics and feedback algorithms, such as excitation-damping measurements, betatron and synchrotron tune measurement, and automated tuning. The lack of logic resources in the current SLS Virtex-2 hardware limits the scalability and modernization of its algorithms.

Filling Pattern Feedback (FPFB) Systems

Figure 7 shows the measurement results of the bunch charge and arrival time obtained at the SLS storage ring. Figure 7a compares the bunch charge measurement of the RFSoC implementation against the existing system presented in [4] and with a soft X-ray photon counting system of the SLS PolLux beamline described in [5]. Figure 7b compares the bunch arrival-time measurements for different methods, and Fig. 7c compares the system performance using the PolLux system as a reference [5].

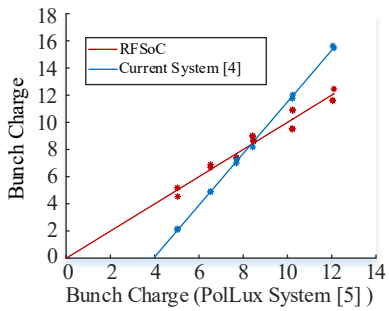

Figure 8: Linearity of the bunch charge measurement for current and RFSoC system, measured at the SLS ring.

The linearity of the bunch charge measurement was evaluated by measuring the charge of a single bunch for different bunch charges with three different systems: The current system [4], the RFSoC, and the PolLux system. The latter is used as a reference for the other systems due to its superior linearity and negligible offset. Figure 8 shows that the RFSoC has a smaller offset than the current system [4] and good linearity. The noise of the RFSoC system can be further improved by averaging longer than the present 128 µs.

For the filling pattern measurement using the RFSoC, the algorithms to calculate bunch charge and bunch arrival-time have been implemented in Python, running offline on a PC. As a next step, we will implement the data processing algorithms in firmware and real-time software on the RFSoC and close the feedback loop. Moreover, we plan to reduce systematic errors in the RFSoC-based filling-pattern measurement. This includes minimizing the impact of reflections on the long cables (from BPM to electronics) on the measurement result.

CONCLUSION

We have evaluated the suitability of RFSoC technology for implementing the MBFB and FPFB of SLS 2.0. While porting the functionality of the existing MBFB implantation to the newer technology, our tests show that the RFSoC meets the requirements for an MBFB system, providing additional resources for future advanced features not feasible with our current SLS hardware. Regarding the FPFB, we have implemented and successfully tested bunch charge and bunch arrival-time measurement using the RFSoC using raw button BPM sum signals. Performance comparisons with the existing systems show that the RFSoC is adequate to measure the filling pattern and has the resources to close the feedback loop by controlling injection and gun charge in real-time. Finally, for both systems, direct sampling of BPM signals and kicker driving is envisaged, using the fast ADCs and DACs of the RFSoC with new simplified analog pre- and postconditioning.

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